SPECIFICATION AMENDMENTS

Please amend the paragraph beginning on page 4, line 10 as follows:

Referring to Figure 1, the L1 cache 12 may be connected by a high bandwidth link to the L2 cache 14. In accordance with one embodiment of the present invention, the L2 cache may be a unified L2 cache. In another embodiment of the present invention, a single core or two more cores may be utilized in systems with separate L2 caches for instructions and data. The L1 cache 12 may include an instruction cache 16, a pipeline 18 and a data cache 20. Two separate L1 caches 14a and 14b may be provided in one embodiment. As a result, cache management logic, snooping support, debugging and monitoring mechanism ~~mechanisms~~ and virtual-to-physical translation may be removed from the L1 caches while still supporting, by a mechanisms in the L2 cache, L1 cache coherency, trace, breakpoints, performance monitoring and virtual memory in the L2 cache 14 as indicated in block 22.

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